Error Analysis of Overlay Compensation Methodologies and Proposed Functional Tolerances for EUV Photomask Flatness

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ABSTRACT

Due to the impact on image placement and overlay errors inherent in all reflective lithography systems, EUV reticles will need to adhere to flatness specifications below 10nm for 2018 production. These single value metrics are near impossible to meet using current tooling infrastructure (current state of the art reticles report P-V flatness ~60nm). In order to focus innovation on areas which lack capability for flatness compensation or correction, this paper redefines flatness metrics as being "correctable" vs. "non-correctable" based on the surface topography's contributions to the final IP budget at wafer, as well as whether data driven corrections (write compensation or at scanner) are available for the reticle's specific shape.

To better understand and define the limitations of write compensation and scanner corrections, an error budget for processes contributing to these two methods is presented. Photomask flatness measurement tools are now targeting 6σ reproducibility <1nm (previous 3σ reproducibility ~3nm) in order to drive down error contributions and provide more accurate data for correction techniques. Taking advantage of the high order measurement capabilities of improved metrology tooling, as well as computational capabilities which enable fast measurements and analysis of sophisticated shapes, we propose a methodology for the industry to create functional tolerances focused on the flatness errors that are not correctable with compensation.

Keywords: Flatness, EUV, Compensation, Overlay, Image Placement, UltraFlat, Functional Tolerance

1. INTRODUCTION

The 2013 ITRS[1] specifies that for the N7 node, overlay requirements will be less than 3.4nm. Due to the impact that mask flatness has on image placement at wafer, the industry has worked to establish specifications that enables out of plane distortion (OPD) and in plane distortion (IPD) levels that still can be accommodated within the ITRS image placement error (IPE) budget. This paper seeks to establish the contributing factors to IPE and the compensation methods used to mitigate them, with the belief that a more thorough understanding of such errors can drive specifications towards functional tolerances that constrain values which lack compensation capability rather than holding polishers to the proposed single scalar metrics. Without the implementation of such correction methodologies, the overlay specifications have the potential to pose an insurmountable burden, and so we propose a more pragmatic approach to flatness specifications based on factors that directly cause additional error to image placement and overlay. With the implementation of write compensation, a highly accurate file containing photomasks topography can be fed to the write tool, and whatever features remain after correction (the non-correctable portion) may require the industry to create or maintain tighter tolerances on these features.

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Process developments from blank manufacturers have greatly decreased flatness and bow contributions to the reticle, however the processes used can induce spatial frequencies that leave the final reticle flatness above the required specifications, impacting final image placement/overlay, and ultimately wafer yield. Write compensation[2-6] remains a promising methodology to mitigate these flatness errors, however understanding the capabilities and limitations of this approach are necessary in order to meet future overlay specifications.

1.1 EUV Flatness Definition

It is important to note that the flatness specifications for EUV masks differ from those of optical photomasks[1]. Optical photomask flatness is reported as the difference between the highest and lowest point on the reticle surface following the removal of the least squares plane. The dominant factor in the second order is film stress, which for EUV lithography is removed during the scanners clamping process[7]. For EUV masks the flatness data is fitted with a 2nd order polynomial (equation 1), which is then removed from the raw flatness data. The final P-V flatness is then determined from the residual of that resulting surface following the removal of the second order fitted polynomial. The quality area for the flatness calculation is the pattern area (132x104mm). Since pattern rotation is used for defect mitigation for EUV masks it is necessary to apply a quality area that covers both possible orientations, X and Y.

ITRS Flatness Calculation

$$Z_{fit} = a + bX + cY + dXY + eX^2 + fY^2 \quad (1)$$

$$Z_{Front_Residuals} = Z_{Front} - Z_{Fit_Front} \quad (2)$$

$$Flatness_{ITRS} = Z_{Residuals}[Max] - Z_{Residuals}[Min] \quad (3)$$

An example of the global flatness calculation for an EUV mask is shown below in Figure 1 for the measurement of the backside of an uncoated EUV reticle. The bow and slope specifications are calculated over a 142x142mm area as specified by the ITRS. The bow is the amplitude of the best fit sphere over the 142x142 area, and is calculated from the raw data. The slope is calculated only for the backside of the mask, and is reported as the maximum angular variation calculated over 20x20mm window stepped across the 142x142mm area.

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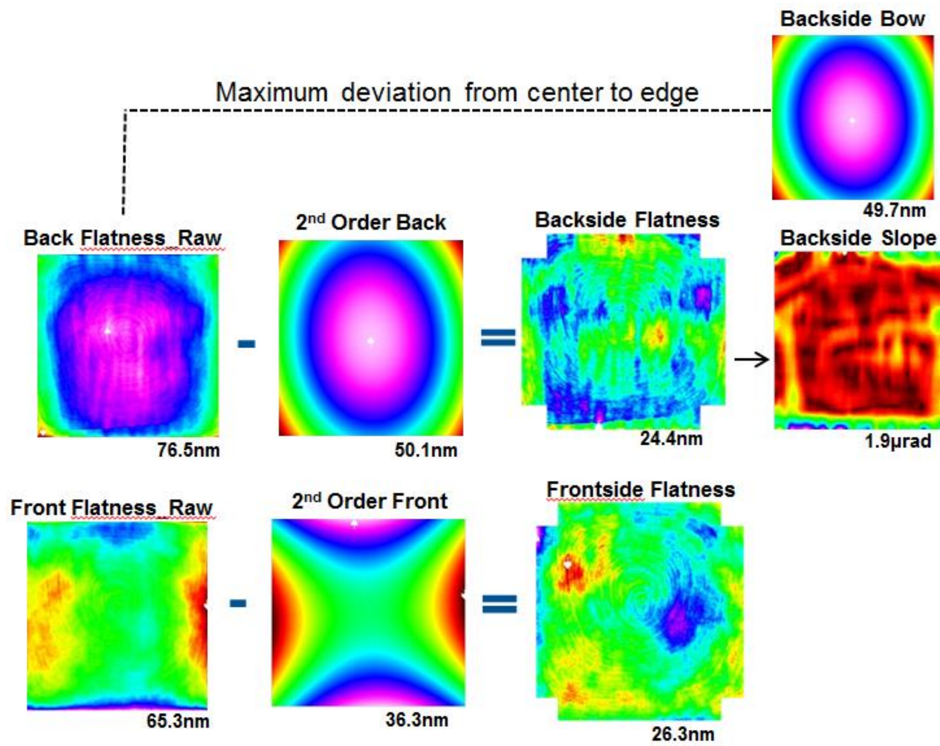

Figure 1: Current method of global flatness calculation as described by the ITRS

1.2 OPD and IPD

Out of plane distortion occurs when the patterned plane of the mask is shifted, resulting in incoming incident rays traversing through an additional amount of space, and offsetting the final pattern. This height variation can be caused by the bow of the reticle, either from the blank or from non-uniform chucking, and can also occur due to variations in the thickness of the photomask. The relationship between the pattern shift at wafer and the reticles height variation during chucking is shown in Figure 2 with the magnitude calculated in equation (4).

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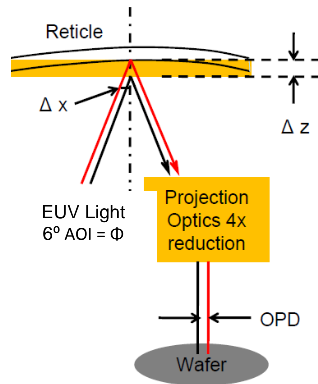

Figure 2: OPD schematic example from photomask non flatness[3]

$$\Delta x = \Delta z * \tan \emptyset * M \qquad (4)$$

In-plane distortion is caused by differences in the chucking mechanisms between the print tools and the scanner. The location of the pattern features shift during chucking depending on the clamped state of the mask. The direction and magnitude of this shift depends on the location of the neutral surface, as well as the slope of the reticle surface and is described in Figure 3 with the magnitude indicated in equation (5).

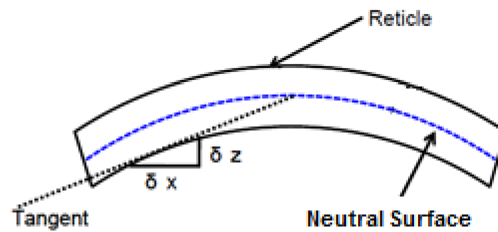

Figure 3: Photomask IPD schematic[3]

$$\Delta x = k * \frac{\partial z}{\partial x} * M * T \qquad (5)$$

The location of the neutral surface (NS), k in equation (5), is typically shown as some fraction of the photomask thickness, T, and is dependent on the individual stresses of each layer on both the front and the backside of the photomask[2]. The neutral surface will shift during mask fabrication, so accurate models must be developed in order for correction tables to be successfully implemented[4].

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As the industry pushes forward, extending EUV technology capabilities, the necessity for larger acceptance angles has prompted the application of anamorphic lenses as a solution to enable better resolution without having to drastically decrease field size. The use of 8x reduction optics would favorably impact OPD and IPD as each of these distortions scale with the magnitude of the reduction optics, however only the scan axis will be reduced by 8x while the other axis will remain at 4x. Since the substrate orientation is currently determined by defect avoidance it is unlikely that the rotation of the mask would be taken into consideration for flatness related errors, in addition to the fact the scan axis orientation is unknown at the time of blank flatness measurements.

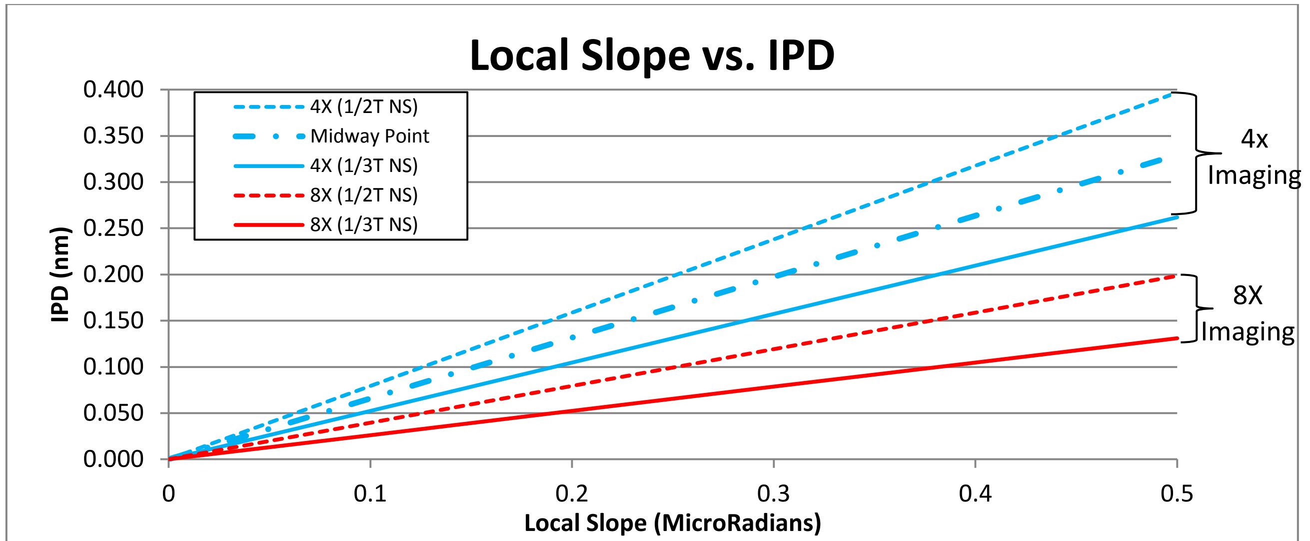

Figure 4: The location of the neutral surface, as well as the magnitude of the reduction optics impacts the resulting IPD (*the midway point is depicted here for illustration purposes in section 2.1)

1.3 Straw Man Budget

The ITRS specifies a node's overlay requirement as some percentage of a technology's minimum half-pitch feature size. Of that minimum overlay requirement, some percentage of the error is allocated to OPD and IPD in the forms of flatness and slope specifications.

The 2013 ITRS initially proposed an 8x magnification change for insertion starting in 2019 (17nm node). With this magnification, the road map calculates the flatness and backside slope limits to be 29nm and 1.0 μrad respectively. These calculations however are based on the 8X magnification, and not anamorphic magnification, which has 8x magnification in the scan axis only. As discussed in previous sections, it is unlikely that topography related specifications will be broken into X and Y components. As such, the industry's topographic specifications will need to be based off the 4x axis since it is the more stringent of the two magnifications.

ASML's NXE scanner roadmap for sub 8nm resolution[8] also shows more aggressive overlay requirements for EUV's lower nodes, with the 13nm node requiring overlay < 1.1nm. Extending the latest published ITRS specifications with the current NXE technology road map, a straw man budget for proposed flatness, and slope specifications is shown below in Table 1 using the same calculations as the ITRS.

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Node	Resolution		2013 ITRS	2013 ITRS No Mag Change	ITRS+ NXE RoadMap
N10	22nm	**Budgeted Overlay (nm)**	**4.4**	**4.4**	**3.0**
		Image Placement (nm)	2.6	2.6	1.8
		Flatness (nm)	25.0	25.0	17.1
		Slope (urad)	0.8	0.8	0.6
N7	16nm	**Budgeted Overlay (nm)**	**3.4**	**3.4**	**1.5**
		Image Placement (nm)	3.0	1.9	0.9
		Flatness (nm)	28.9	18.0	8.6
		Slope (urad)	1.0	0.6	0.3
N5	13nm	**Budgeted Overlay (nm)**	**2.6**	**2.6**	**1.4**
		Image Placement (nm)	2.3	1.6	0.8
		Flatness (nm)	22.3	15.0	8.0
		Slope (urad)	0.7	0.5	0.3
N5	10nm	**Budgeted Overlay (nm)**	**2.0**	**2**	**1.2**
		Image Placement (nm)	1.8	1.2	0.7
		Flatness (nm)	17.2	11.0	6.9
		Slope (urad)	0.6	0.4	0.2
N3	7nm	**Budgeted Overlay (nm)**	**1.4**	**1.4**	**1**
		Image Placement (nm)	1.3	0.9	0.6
		Flatness (nm)	12.1	8.0	5.7
		Slope (urad)	0.4	0.3	0.2

Table 1: Photomask topography strawman budget based on 2013 ITRS and NXE roadmap

The values shown in Table 1 depict the extrapolation of the previously published ITRS results in combination with the NXE technology roadmap. These specifications exemplify flatter results than the current champion masks being produced for EUV development and manufacturing.

2. PROPOSED FLATNESS METHODOLOGY

There are a number of factors that feed into the budgeted overlay. Figure 5 below shows the key contributors to the overall requirements broken down by where in the process they take place. This paper focuses on the highlighted segments of the figure.

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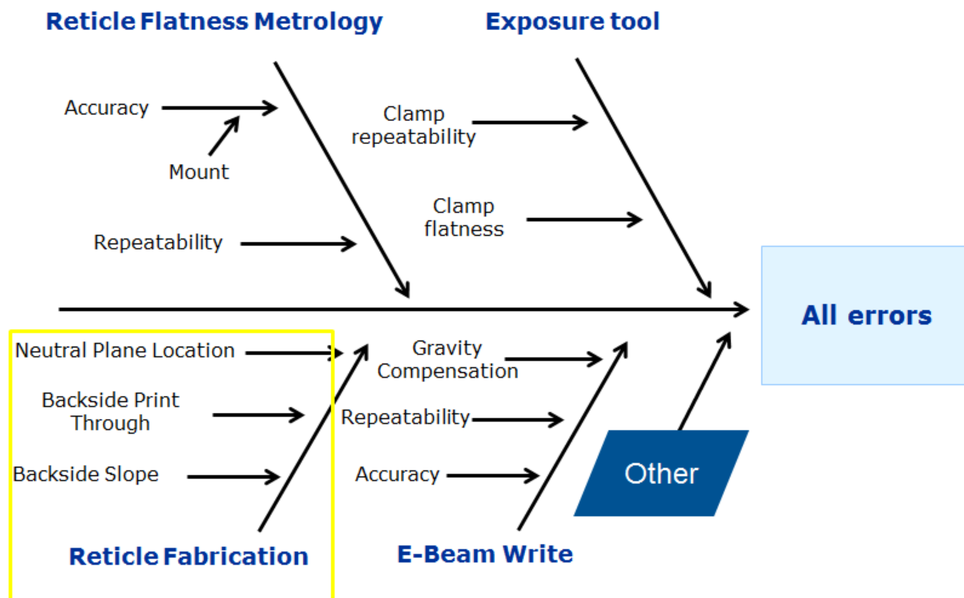

Figure 5: Fishbone diagram showing potential error contributors for overlay

PROPOSED FLATNESS METHODOLOGY

The current ITRS flatness calculations and tolerances are built around the assumption that write compensation will not be used. As shown in the roadmap discussion above, the industry is unlikely to be able to achieve the extremely tight levels of flatness performance required for N7 insertion, thus becomes clear that write compensation will be required. With the employment of write compensation, the requirements for flatness change significantly. This section will detail the proposed breakdown of flatness information that feeds into write compensation, and the portion that must be controlled during substrate polishing.

2.1 Calculations

The current methodology for global flatness calculations takes raw data from the surface of interest (front or back) and removes the 2nd order fit as a way to emulate the chucking process and better simulate the final chucked flatness of the photomask.

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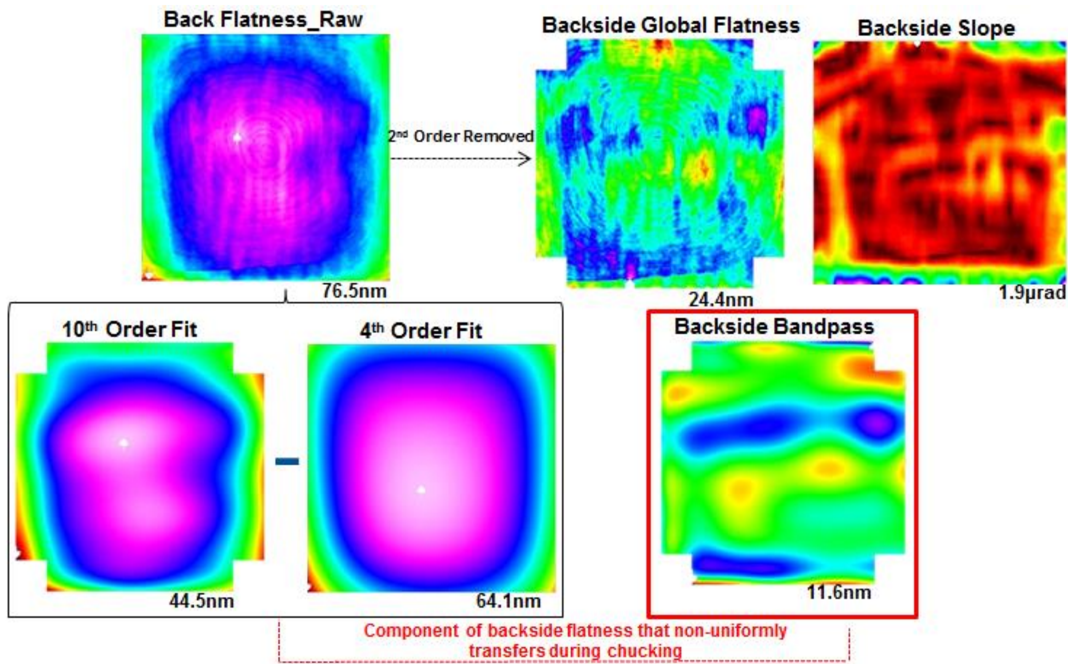

Figure 6: Proposed back side flatness calculation based on bandpass filtering for transferable spatial frequencies

Although discrepancies still remain as to what aspect of the backside non-flatness transfers to the front during chucking, multiple studies have demonstrated that all of the backside form up to 4th order should print through to the front side during clamping, and that frequencies falling between 4th and 10th order will print through to some extent[9,10]. Since the portion of the 4th to 10th order does not agree between different calculation methods, it becomes critical to minimize these backside features.

By focusing efforts on driving these mid-spatial frequencies (4th order to 10th order Legendre terms) down it is then possible to decrease their potential error in write compensation. This is shown in Figure 6 where the backside bandpass map describes these mid-spatial frequencies. We suggest that the ITRS+ NXE roadmap flatness tolerance for the backside be applied only to this back side bandpass data.

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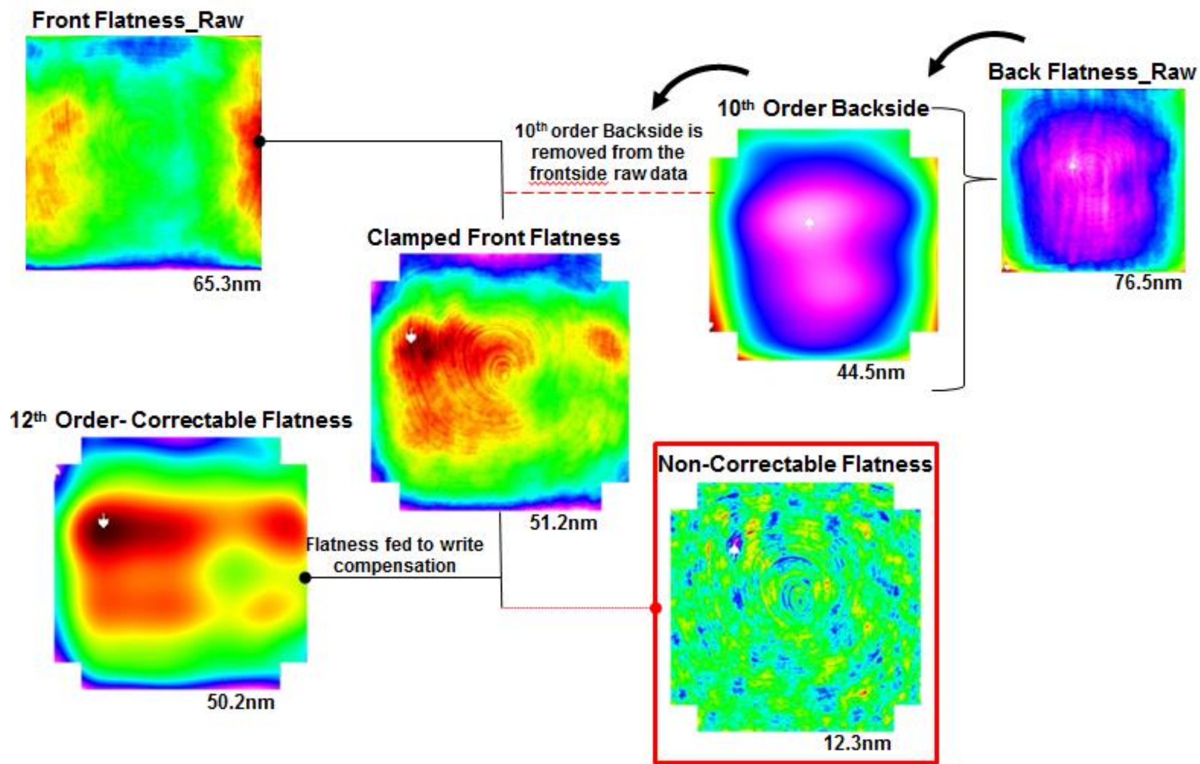

Figure 7: Proposed frontside flatness calculation methodologies based on write compensation capabilities

The front side data therefore includes the 10th order Legendre fit of the backside data in its final results to simulate the clamping state. When analyzing the simulated clamped front side topography the majority of the surface can be well characterized by a 12th order Legendre polynomial fit. Any higher order, and the change in the magnitude of the residual has little impact as the remaining structure is of a much higher frequency content, which likely cannot be write compensated. For this reason, we recommend using the 12th order Legendre fit as a feed forward for the write compensation, and assign the ITRS + NXE roadmap flatness specifications to the residual of this fit. This analysis is outlined in Figure 7. The residuals from this 12th order fit then constitute the non-correctable portion of the front side flatness, and so will need to be tightly monitored and controlled in order to limit their contribution to the final IP error at wafer.

2.1 Reticle Fabrication Error Analysis

Bending of the mask due to film stress contributes to IPD and overlay error at wafer since the shape of the mask in the e-beam writer differs from the clamped shape resulting from the electrostatic chuck (ESC). The precise location of the neutral plane depends upon the specific film stack of the reticle and must be calculated prior to patterning since compensation is applied before e-beam write. Changes to the film stack affect the location of the neutral surface as well as the stress distribution. The location of the neutral surface, the magnification of the system, and most importantly the magnitude of the backside slope all contribute to the final IPD, and as such must be minimized when possible either through process development or compensation.

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For the **N7** node (16nm HP) the local slope must be less than 0.3μradians. As discussed in previous sections, the IPD resulting from this slope is dependent on the location of the reticles neutral surface, and any errors in the calculation of the location of this surface would add additional IPE at wafer. At this point in time, there remains uncertainty around the "correct" value for the location, however most models place the surface somewhere between 1/2T and 1/3T[4]. For the sake of our critical budget calculations shown below in Table 2, we have placed the NS at the midway point between these two values (Figure 4). At this location, assuming the 0.3 μradian specification has been met, the IPD value is 0.2nm. The largest possible IPE from this NS location is the difference between the two extremes of the possible NS positions (1/2 and 1/3) which is ± 0.04nm. This error would be included in the data file generated for the write tool; however it is a relatively small contribution.

Backside print through continues to be a concern due to the fact that current reported results still show deviations between analytical predictions and FEA (either of which would be used for compensation). The general consensus is that higher spatial frequencies, greater than 10th, order are not transmitted[9, 10], however lower frequencies have the potential to be fully transmitted depending on specific material properties. In order to better accommodate the non-reproducible portion of backside print through, the industry would be best served to address 4nd through 10th order spatial frequencies present on the backside of the mask. The backside print through and slope reported in Table 2 were determined using the previously prescribed method of using a bandpass filter (10th order- 4nd order) and assuming the residual fully prints through to the front side of the mask. To perform these calculations, as well as those for the front side error contribution, an EUV substrate with roughly 70nm of shape was used.

Resulting Image Placement Error	Value at Reticle (nm)	Value at wafer (nm)	correctable (nm)	non-correctable
Reticle Fabrication				
Backside Slope (IPD) (μradians)	0.30 μradians	0.24	0.20	0.04
Backside Print through (OPD)	24.40	0.61	0.61	0.29
Frontside Flatness (OPD)	26.30	0.66	1.26	0.31

Table 2: IPE analysis for reticle fabrication error contributors for write compensation

Table 2 summarizes potential IP errors which could result for different steps from reticle fabrication through final exposure in the scanner. Compensation techniques may be limited in scope for certain errors, and so factors which contribute such errors must be driven down through tightened tolerances, and greater process development. The values reported are from current literature, empirical data, or some combination of both. It should be noted that much of the research conducted on these issues occurred around 2009, and many of these numbers reported could be outdated. It will be necessary for the industry to re-investigate some of these contributors and determine their current impact to the IPE.

3. SUMMARY

Using the new proposed flatness methodology demonstrated in this paper it is possible for polishers to reach the IPE budget needed for photomask blank flatness while adhering to the industry's strict IPE budget. Under the current specification for the ITRS, polishers have been held accountable to reach single digit nanometer values for reticle flatness, a feat which they are unlikely to accomplish at a reasonable cost. With the adoption of write compensation, these specifications can be drastically loosened on the substrate and will hold polishers to set of metrics that focus on features which cannot be compensated at write. Rather than having to drive the global flatness of the entire reticle down,

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the substrate non-flatness that must be considered is then the “non-correctable” component which is dominated by mid to high spatial frequency features on the front side induced during polish, as well as the non-flatness of the 10th-4th order backside fitted flatness results which add unpredictability to the final IP error at wafer. In theory there should be room to loosen the specifications for slope as well, however at this point in time we do not have a proposal for the magnitude to which these specifications could be relaxed. Consideration must also be given to the fact that although flatness induced errors may be mitigated by write compensation, OPD will still likely be limited by the depth of focus of the scanner.

In this paper we have discussed the reticle fabrication process’ contributions to overlay, however the rest of the contributors on Figure 4 need to be characterized, and focus further work on the largest remaining error sources. Research is currently being conducted further understanding errors related to the exposure tool, flatness metrology and e-beam write, and will be provided in future publications.

Write compensation is a key tool for enabling EUV’s advancement and successfully achieving continually tightening flatness IP and overlay specifications. The use of high accuracy flatness data for feed forward corrective pattern placement has historically shown promising results. By understanding what aspects of substrate topography can and cannot be corrected at mask write, a better set of tolerances can be established that enable the industry to meet all the stringent requirements for successful adoption of EUV to high volume manufacturing.

4. ACKNOWLEDGEMENTS

We wish to thank John Zimmerman of ASML for extending his knowledge and expertise on this subject matter. Without all of the hours of his contributed efforts this paper would not have been possible.

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